REMARKS

Favorable reconsideration of this application is respectfully requested in view of the foregoing amendments and the following remarks.

By this Amendment, Figure 5 is amended, claim 9 is canceled and claims 4, 7 and 10 are amended. The subject matter of the amendments to the claims is fully supported in the specification as filed. No new matter is added. Thus, claims 4-8 and 10 are currently pending in the application and subject to examination.

Amendment to the Drawings

The Applicants have amended Fig. 5 to correctly place previously misplaced labels "61a MEMORY ARRAY" and "61b DECODING CIRCUIT". No new matter is added.

Claims 4-8 and 10 Recite Patentable Subject Matter

In the Office Action mailed May 4, 2005, claims 4-10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U. S. Patent No. 6,178,127 B1 to Haraguchi in view of U.S. Patent No. 6,735,727 B1 to Lee. It is noted that claim 9 has been canceled and claims 4, 7 and 10 have been amended. To the extent that the rejection remains applicable to the claims currently pending, the Applicants hereby traverse the rejection, as follows.

Claim 4, as amended, recites, in part:

> a redundant circuit, located proximate to the drive circuit of each of the plurality of subblocks and comprising a volatile storage circuit, for substituting one of the lines including the redundant line of the corresponding subblock for a defective line in that subblock according to the state of the volatile storage circuit;

> common signal lines for connecting the defective line information store circuit and the redundant circuit corresponding to each subblock and for connecting the address input circuit and the drive circuit of each subblock to deliver the address signal input; and
>
> a supply circuit for transferring the defective line information from the defective line information store circuit to the volatile storage circuit in the redundant circuit corresponding to each subblock via the common signal lines.

Thus, the semiconductor memory device claimed in claim 4 has a distinctive feature of transferring defective line information from a defective line information store circuit to a volatile storage circuit in a redundant circuit via common signal lines. More specifically, the redundant circuit, which is located proximate to the drive circuit of each of the plurality of subblocks, has a volatile storage circuit. In addition, the common signal lines of claim 4 connect the defective line information store circuit and the redundant circuit corresponding to each subblock and connect the address input circuit and the drive circuit of each subblock to deliver the address signal input. Claim 4 further recites a supply circuit for transferring the defective line information from the defective line information store circuit to the volatile storage circuit in the redundant circuit corresponding to each subblock via the common signal lines. Thus, in claim 4, the common signal lines connect the address input circuit and the drive circuit of each subblock to deliver the address signal input and carry the defective line information. Therefore, the signal line that connects the address input circuit to the drive circuit is also used to connect the supply circuit, which supplies information stored in the defective line information store circuit to the redundant circuit. As such, the present invention of claim 4 results in at least the advantages of simple structure and operation of a semiconductor memory device.

The Applicants respectfully submit that none of the cited art of record, alone or in combination, discloses or suggests at least the above combination of features recited in claim 4, as amended.

Haraguchi discloses a plurality of memory blocks with redundancy for repair of defective columns. Haraguchi provides replacement column address program circuits (RAPs) and replacement I/O program circuits (RIPs) for storing repair information. All RAPs and RIPs are connected directly to memory blocks to provide repair information. This reference does not, however, disclose or suggest at least the combination of features of a redundant circuit, located proximate to the drive circuit of each of the plurality of subblocks and comprising a volatile storage circuit, for substituting one of the lines including the redundant line of the corresponding subblock for a defective line in that subblock according to the state of the volatile storage circuit; common signal lines for connecting the defective line information store circuit and the redundant circuit corresponding to each subblock and for connecting the address input circuit and the drive circuit of each subblock to deliver the address signal input; and a supply circuit for transferring the defective line information from the defective line information store circuit to the volatile storage circuit in the redundant circuit corresponding to each subblock via the common signal lines, as recited in claim 4, as amended.

In rejecting claims 4-10, the Office Action admits that Haraguchi fails to disclose the redundant circuit including a storage circuit as recited in claim 4, and asserts that Lee cures this deficiency of Haraguchi. However, the redundancy selection circuit 300 (FIG. 4) of Lee has non-volatile flash EEPROM memory (see Lee at column 8, lines 30-33), whereas the redundant circuit of the present invention has a volatile storage circuit.

Moreover, Lee fails to disclose or suggest transferring defective line information from a defective line information store circuit to a volatile storage circuit in a redundant circuit via common signal lines that are also used to carry address signals, as set forth in claim 4. For at least these reasons, the Applicants submit that Lee neither discloses nor suggests at least the combination of a redundant circuit, located proximate to the drive circuit of each of the plurality of subblocks and comprising a volatile storage circuit, for substituting one of the lines including the redundant line of the corresponding subblock for a defective line in that subblock according to the state of the volatile storage circuit; common signal lines for connecting the defective line information store circuit and the redundant circuit corresponding to each subblock and for connecting the address input circuit and the drive circuit of each subblock to deliver the address signal input; and a supply circuit for transferring the defective line information from the defective line information store circuit to the volatile storage circuit in the redundant circuit corresponding to each subblock via the common signal lines, as recited in claim 4, as amended.

For all of the above reasons, the Applicants submit that neither Haraguchi nor Lee, alone or combined, discloses or suggests at least the combination of a redundant circuit, located proximate to the drive circuit of each of the plurality of subblocks and comprising a volatile storage circuit, for substituting one of the lines including the redundant line of the corresponding subblock for a defective line in that subblock according to the state of the volatile storage circuit; common signal lines for connecting the defective line information store circuit and the redundant circuit corresponding to each subblock and for connecting the address input circuit and the drive circuit of each

subblock to deliver the address signal input; and a supply circuit for transferring the defective line information from the defective line information store circuit to the volatile storage circuit in the redundant circuit corresponding to each subblock via the common signal lines, as recited in claim 4, as amended.

The Applicants respectfully submit that claim 4, as amended, is allowable over the cited prior art. As claim 4 is allowable, the Applicants submit that claims 5-8 and 10, which depend from claim 4, are allowable for at least the same reasons as claim 4, as well as for the additional subject matter recited therein.

Applicants respectfully request withdrawal of the rejection of claims 4-8 and 10.

Conclusion

For all of the above reasons, it is respectfully submitted that claims 4-8 and 10 are in condition for allowance and a Notice of Allowability is earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is invited to contact the undersigned representative at the telephone number listed below.

In the event this paper is not considered to be timely filed, the Applicants hereby petition for an appropriate extension of time. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300 referencing client matter number 107337-00053.

Respectfully submitted,

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Enclosures: Replacement Sheet (Figure 5)

AMENDMENTS TO THE DRAWINGS

The attached sheet of drawings includes changes to Figure 5. This sheet replaces the original sheet including Fig. 5. In Figure 5, reference numeral 61a along with corresponding label "MEMORY ARRAY" has been exchanged with reference numeral 61b and corresponding label "DECODING CIRCUIT". The reference numerals and labels for the memory array 61a and the decoding circuit 61b of Fig. 5 were switched in order to correctly identify the memory array and the decoding circuit. No new matter has been added.

Attachment: Replacement Sheet